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- (71) Applicant (for all designated States except US): ERICS-SON INC. [US/US]; 7001 Development Drive, Research Triangle Park, NC 27709 (US).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): WILCOX, Bruce, Emerson [US/US]; 118 Trailview Drive. Cary, NC 27513 (US). DOUGLAS, Mark, Gordon [CA/US]; 327 Bond Lake Dr., Cary, NC 27513 (US).
- (74) Agent: BENNETT, David, E.; Coats & Bennett, PLLC, P.O. Box 5, Raleigh. NC 27602 (US).

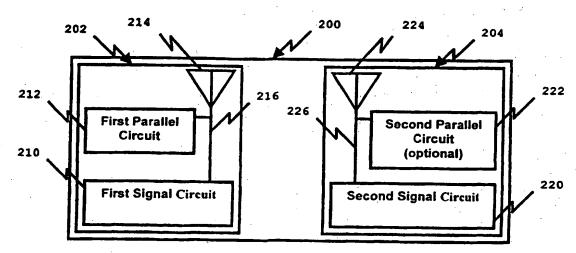
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(54) Title: MULTIPLE ANTENNA IMPEDANCE OPTIMIZATION



(57) Abstract: A multiple antenna mobile communication device, such as a cellular telephone, having multiple radios and multiple antennas located in close proximity to each other uses a parallel tuning circuit to optimize the isolation between the antennas. The parallel tuning circuit can include multiple impedance matching circuits to match the impedance in multiple frequency bands or isolating antennas.



WO 01/7184

MULTIPLE ANTENNA IMPEDANCE OPTIMIZATION

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates in general to multiple antenna impedance optimization. In particular, the present invention relates to a method and apparatus for impedance transformation between two antennas in close proximity to each other.

2. BACKGROUND

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Cellular radiotelephones, combined cellular and satellite radiotelephones, and other wireless communications devices often employ two or more antennas, each of which are connected with a separate radio. Due to the limited space on most wireless devices, it is highly desirable to locate these antennas close together. However, without isolating the electromagnetic coupling between the antennas, there is a limitation on how closely the antennas can be spaced from each other. Coupling between the antennas creates several problems, including: reducing the gain of each antenna because some of the radiated power from each antenna is absorbed by the other antenna; creating tuning and impedance mismatches in each antenna, causing mismatch loss and/or lower impedance bandwidth; mixing of signals which can result in spurious emissions; and damaging of a receiver of one radio by a strong signal transmitted from the other radio.

Multiple antenna isolation can be achieved by placing a circuit in series between the radio transmitter and its antenna. Examples of series circuits are filters, switches, and directional attenuators. A series filter circuit presents a lower insertion loss across the frequency band of the first antenna and a higher insertion loss across the frequency band of the second antenna. A switch is closed when its antenna is in use and open when the second antenna is in use. The switch should be located near the base of the antenna to ensure that the

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length of transmission line between the switch and the antenna base does not transform the open circuit impedance at the switch to some other impedance as described in U.S. patent 5,060,293. A filter in combination with a directional attenuator provides antenna isolation as described in US Patent 5,815,805. A shortcoming of filters is the insertion loss, which can be significant. A shortcoming of using a switch is that the switch must be located very close to the base of the antenna.

Multiple antenna isolation can be achieved by creating a canceling signal (interference signal) in a third antenna that cancels the signal from the second antenna, as described in U.S. Patent 4,233,607. This method requires additional hardware including an antenna and a signal generator signal to generate the canceling signal. Multiple antenna isolation can also be achieved by anti-phase combination of signals as described in U.S. Patent 5,264,862. Multiple antenna isolation can also be achieved by using uncorrelated radiating modes as described in Canadian patent 2,095,304. Using uncorrelated radiating requires the two antennas to be oriented in one of a limited number of possible orientations to create orthogonal polarization and radiation patterns. Such limited orientations prohibit using this method in many applications with physical space constraints. Further, this method can be applied to at most three antennas. Multiple antenna isolation can also be achieved by arranging narrow beamwidth antennas sectorally such that their radiation patterns do not overlap as described in U.S. patent 5,771,449. However, sectoral arrangement is impractical in most applications with size constraints, such as cellular telephones.

A wide band antenna can be used with a frequency diplexing circuit to separate the communication signals into the appropriate frequency bands. For example, a single antenna in a cellular telephone can be used to simultaneously transmit and receive cellular telephone calls. These designs have several disadvantages. First, a single feed point wide band antenna with multiple radios attached is difficult to design. Second, the frequency diplexing circuit exhibits high insertion loss. Higher insertion loss causes lower communication quality and

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higher battery current consumption rates, which decreases the operational time in battery operated devices.

Alternatively, a multiple pole switching circuit can separate transmit and receive frequency ranges on a wide band antenna. The multiple pole switching circuit has three primary disadvantages: high insertion loss, increased current consumption, and lower linearity. Lower linearity is a result of an increase in spurious emissions during transmitting and an increase in spurious input signals during receiving.

A dual-mode phone operates on two modes, usually digital and analog. For example, a dual-band phone operates on the cellular band (800MHz) and the PCS band (1900MHz).

A brief summary of the mobile standards commonly used includes:

Multiple access techniques: FDMA allows multiple stations to use different frequencies within an operating frequency channel. Time Division Multiple Access (TDMA) allows mobile stations to use the same frequency, but signals are separated by time slots. Code Division Multiple Access (CDMA) allows multiple mobile stations to use the same frequency, but signals are separated by unique digital codes. CDMA uses spread spectrum techniques. Personal Communication Services (PCS) is a digital communication standard that is commonly referred to as the 1900MHz (1.9GHz) band. However, the band is actually from 1850MHz to 1990MHz.

Operating modes that use one or more multiple access techniques:

Advanced Mobile Phone System (AMPS) is an analog system used in the United States for cellular telephones. AMPS uses Frequency Modulation (FM) and the FDMA air interface. The frequency band for AMPS is 824MHz to 849MHz and 869MHz to 894MHz. Each channel is 30KHz wide. Narrow-band Advanced Mobile Phone Service (NAMPS) operates with the 30KHz channels used in AMPS divided into three 10KHz channels. Global System for Mobile Communications (GSM) is a European standard for digital wireless communications. GSM uses a combination of FDMA and TDMA. GSM divides the 25MHz band into 124 frequencies of 200KHz each. GSM uses 8 time slots

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rotated at 214 times per second. GSM in the United States uses the PCS band (1900 MHz). Digital Advanced Mobile Phone System (DAMPS), like GSM, uses TDMA and FDMA. However, DAMPS uses 3 time slots rotated at 50 times per second. Bluetooth is a specification for short range radio links between mobile PCs, mobile phones and other portable devices. Bluetooth radios operate in the unlicensed ISM band at 2.4 GHz and use a time-division duplex scheme for full-duplex transmission. The range of Bluetooth is only from 10 cm to 10 m, but can be extended to 100 m. Thus, Bluetooth is useful as a data link between a cellular telephone and a near by computer. Mobile satellite telephones, communicate via satellites instead of cellular base stations. Such phones are available from IRIDIUM and GlobalStar.

Figure 1 shows a typical prior art multiple antenna system 100 with two radio antenna systems 102, 104 that uses series circuits. The radio antenna system 102 includes a radio 110, an antenna 114, and a series circuit 112, in series between the radio 110 and antenna 114. The radio antenna system 104 includes a radio 120, an antenna 124, and a series circuit 122 in series between the radio 120 and antenna 124.

SUMMARY

The present invention is defined by the following claims, and nothing in this section should be taken as a limitation on those claims. By way of introduction, the preferred embodiments described below include a mobile communication device, such as a cellular telephone, with multiple radios and antennas located in close proximity to each other. A parallel tuning circuit connectable to the signal path adjusts the impedance in an antenna in order to reduce the interference (coupling) between the antennas. The parallel tuning circuit can include multiple impedance matching circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram representing a prior art system with two radio antenna systems in close proximity using a series tuning circuit;

Figure 2 is a diagram representing a system with two radio antenna systems in close proximity incorporating a parallel tuning circuit;

Figure 3 is a diagram representing a radio antenna system incorporating a parallel tuning circuit;

Figure 4 is a schematic diagram of a parallel tuning circuit; and Figure 5 is a circuit diagram representing an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention, in one embodiment, can incorporate a cellular telephone with a first antenna and an additional antenna and radio for communicating with a personal computer(PC) using the Bluetooth interface. Since antenna interference (coupling) in a multiple antenna system can de-tune the antenna, causing damage to the radio attached to the non-transmitting antenna, and other problems, antenna isolation is required. Physical isolation is not practical in a handheld device because of space limitations. The present invention includes a parallel impedance circuit that is selectively connected near the base of the first antenna to isolate the second antenna from the first antenna when the second antenna is operational.

Advantages of this invention include reduced power consumption, reduced antenna sizes, the ability to locate multiple antennas closer together, reduced coupling between antennas, reduced feedback in radios, better impedance matching, and reduced spurious emissions.

While a cellular telephone has been used as an example, the present invention can apply to numerous devices, especially small handheld devices with multiple antennas. For example, a Global Positioning System (GPS) unit with a Bluetooth interface, each having their own antenna would need antenna isolation.

Figure 2 is an embodiment of the invention, a multiple antenna system 200 with two antenna systems 202, 204. The first antenna system 202 includes a signal circuit 210, an antenna 214, and a parallel circuit 212 in parallel with the

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signal circuit 210 and antenna 214. The second antenna system204 includes a signal circuit 220, an antenna 224, and optionally a parallel circuit 222 in parallel with the signal circuit 220 and antenna 224. The antennas 214, 224 are located in close proximity (within approximately one wave length or less) to each other. Two antennas are in close proximity when a transmission from one antenna is affected by the presence of the other antenna. The signal circuits 210, 220 can be transmitters, receivers, or transceivers for radios, cellular telephone radios, walkie-talkies, GPS systems or other circuits that transmit and/or receive a signal over an antenna.

The parallel circuit 212 is preferably connected as close to the antenna 214 as practical. By locating the parallel circuit 212 close to the antenna 214, the RF power loss of the transmission path is decreased.

In an embodiment, only the first antenna system has a parallel circuit. In this embodiment, only the antenna system with the parallel circuit is isolated from the other antenna. In an alternative embodiment, both antenna systems 202, 204 are connected with parallel circuits 212, 222.

Also, the parallel circuit can be applied to a multiple antenna system with more than two antennas. For example, a multiple antenna system can have two (2) to ten (10), or more antenna systems located physically close to each other. There is no known practical limit to the number of antennas in the multiple antenna systems implementing the disclosed invention.

In a preferred embodiment, the second signal circuit 220 can generate signals in multiple frequency bands, and the first parallel circuit 212 can maximize the antenna to antenna isolation. The first parallel circuit 212 can include an impedance matching circuit or other tuning circuit. Alternatively, the first parallel impedance matching circuit may be used to indirectly or directly correct the impedance mismatch between the second antenna 224 and the second signal circuit 220.

Optionally, the multiple antenna system 200 can include a second parallel circuit 222 selectively connectable to the second signal path 226. The second parallel circuit 222 can reduce the coupling between the first and second

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antennas 214, 224 by presenting a high insertion loss between the antenna 224 and the signal circuit 220 when the signal circuit 210 is in use and a low insertion loss between the same points when the signal circuit 220 is in use.

It is preferable that the first parallel circuit 212 be connected to the first signal path 216 near the first antenna 214 and create a termination impedance at the input to the first antenna 214 equivalent to an open circuit when the second signal circuit is in use. The first parallel circuit 212 can include active or passive components.

Further, the first parallel circuit 212 can be used to improve the impedance match between the second antenna 224 and the second signal source 220. Because the two antennas 214, 224 are in close proximity with each other, the impedance match of the second antenna 224 is affected by the presence of the first antenna 214. The first parallel circuit 212 can create a terminating impedance in the first antenna 214 that adjusts the impedance match in the second antenna 224. It is preferred that active controls be used to perform this function.

Figure 3 shows an antenna system 300 that includes a first signal circuit 304, such as a radio, connected with an antenna 308 via a transmission line 306. Also, a parallel circuit 302 is selectively connectable to the transmission line 306. In an embodiment, the parallel circuit 302 includes a main switch 310, and one or more secondary switches 314, 318, 322. The main switch 310 connects or disconnects the parallel circuit 302 from the rest of the radio antenna system 300. Each secondary switch 314, 318, 322 connects a tuning circuit 312, 316, 320 to the main switch. The tuning circuits 312, 316, 320 are also called impedance matching circuits. While Figure 3 illustrates one embodiment of the present invention that includes a main switch and a plurality of secondary switches, numerous alternative configurations also achieve the desire result of selectively connecting one or more of the tuning circuits 312, 316, 320 to the transmission line 306.

A tuning circuit, e.g. 312, can include a band tuning circuit. When the first signal circuit 304 is not in use, the band tuning circuit tunes the first antenna 308

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to a specific impedance, such that the antenna to antenna isolation is maximized in a predetermined frequency band.

While a primary purpose of the parallel tuning circuit 302 is to reduce interference between antennas in a multiple antenna system, a parallel tuning circuit can also be used to compensate for external signal interference. External interference can result from a variety of sources including placing a hand near the cellular telephone antenna. Such external interference de-tunes the antenna. It is preferable that such a tuning circuit be automatically connectable to the transmission line 306 to dynamically compensate for the external interference. Optionally, an interference detector or other detector can be used to dynamically connect one or more of the tuning circuits with the first signal path.

In an embodiment, at least one of the plurality of tuning circuits 312, 316, 320 maximizes the isolation between the first and second antennas, and the other tuning circuits maximize the isolation between the first antenna and other adjacent antennas. It is preferred that the tuning circuits 312, 316, 320 match the impedance in multiple frequency bands. In another embodiment, the tuning circuits 312, 316, 320 maximize the isolation between the first and second antennas in various operating environments.

Each of the plurality of impedance matching circuits 312, 316, 320 can be independently selectively connectable in parallel with the other tuning circuits to the transmission line.

The signal circuit 304 can generate and/or receive electromagnetic signals, preferably radio signals or cellular telephone signals. In a multiple antenna system with multiple signal circuits, the signal circuits may generate signals at the same or different frequencies bands.

In an embodiment, the multiple antennas can be formed on a common material, such as a dielectric substrate. The tuning circuit can be created on a single semiconductor or it can be made using micro-electro-mechanical systems ("MEMS") technology. It is preferred that the switches be MEMS switches.

Figure 4 shows an embodiment of a parallel circuit 400 connected with a transmission line 402 with two tuning circuits. The embodiment of a parallel

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circuit 400 is one of many possible embodiments of the parallel circuit 212, 222 (Figure 2), or 302 (Figure 3). For example, RLC circuit 418, diode circuit 412 and variable impedance circuit 420 are equivalent to tuning circuit 312 and switch 314 and RLC circuit 414, diode circuit 410 and variable impedance circuit 416 are equivalent to tuning circuit 316 and switch 318. The parallel circuit 400 includes four RLC circuits 404, 408, 414, 418, three diode circuits 406, 410, 412, and two variable impedance circuits 416, 420. The parallel circuit 400 has three inputs labeled "Enable", "Select 1", and "Select 2". The three inputs control how the parallel circuit 400 affects the signal path. Each RLC circuit 404, 408, 414, 418 includes an inductor, a resistor, and a capacitor, preferably connected in a "T" configuration.

The diode circuits 406, 412, 410 preferably include PIN diodes. PIN diodes are commonly used for switching and attenuating RF (radio frequency) signals. A PIN diode has P-doped and N-doped regions with an undoped, "intrinsic", region in between. When the PIN diode is forward biased to conduct current, it will also conduct a high-frequency signal superimposed on the current, even if the signal is large, with minimal distortion to the high-frequency signal. The PIN diode, used at high frequencies, is similar to a variable resistor, whose resistance decreases as current increases.

Control signals are applied at the Enable, Select 1, and Select 2 terminals. The control signals are generated as desired to control the parallel circuit 400. It is preferred that an automated circuit generate the control signals based on the operating state of the antennas in the multiple antenna system. It is preferred that low leakage bipolar transistor circuits drive the control signals.

Operational Mode/Controls Select 2 Enable Select 1 Floating Floating Transmission Floating 0 Vdc Floating Isolation Band 1 +3.0 Vdc +3.0 Vdc Floating 0 Vdc **Isolation Band 2**

Table 1

Table 1 illustrates an embodiment of the operating modes and the control signals associated with each operating mode for the parallel circuit in Figure 4.

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Table 1 assumes that the parallel circuit 400 (Figure 4) is used in a multiple antenna system such as 202 (Figure 2) or 300 (Figure 3) and that the parallel circuit can isolate two frequency bands "Isolation Band 1" and " Isolation Band 2" as well as allow the signal circuit to transmit a signal. The isolation frequency bands can be any frequency ranges desired.

Since the parallel circuit 400 is used in a multiple antenna system, it is preferred that one of the bands isolate the frequencies used by other antennas. Thus, in a multiple antenna system with three antenna systems, the first antenna system may have a parallel circuit and "isolation band 1" may correspond to the second antenna system's transmitting frequency, and "isolation band 2" may correspond to the third antenna system's transmitting frequency. Isolation band 1 is used in the parallel circuit connected with the first antenna system when the second antenna system is transmitting. Likewise, isolation band 2 mode is used in the parallel circuit 400 connected with the first antenna system when the third antenna system is transmitting. It is preferred that isolation band 1 and isolation band 2 be different frequency ranges. However, they may overlap.

The control signals, Enable, Select 1, and Select 2, can be digitally controlled from a control input circuit. The control input circuit can be manually operated or preferably automatically operated based on the transmit and receive states of each antenna in the multiple antenna system. The control input circuit can sense the states of each antenna and apply appropriate signals to the control inputs to all antennas with parallel circuits. It is preferred that low leakage bipolar transistors drive the control inputs.

The "transmission mode" is used when the antenna system connected with the parallel circuit 400 is transmitting or receiving and the other antennas are not transmitting. When the "transmission mode" is used, the Enable, Select 1, and Select 2 are allowed to float. When all three inputs are allowed to float, the parallel circuit 400 is in "thru" mode and the parallel circuit 400 does not tune the antenna. When the band 1 is to be isolated, the "isolation band 1" mode is used and 3 volts DC is applied to Enable, zero volts is applied to Select 1, and Select 2 is allowed to float. When the band 2 is to be isolated, the "isolation band 2" mode is used and 3

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volts DC is applied to Enable, Select 1 is allowed to float, and zero volts is applied to Select 2. The isolation modes are preferably used on the first tuning circuit when the first antenna is not transmitting and an other antenna is transmitting. The modes and controls of Table 1 also apply to the parallel circuit 504 shown in Figure 5.

Figure 5 is an embodiment of a circuit 500 with a transmission line 506. a quarter wave section ("QWS") 502, and a quarter wave termination circuit ("QWT circuit") 504 also called a parallel circuit. The QWT circuit 504 is an embodiment of the parallel circuit 400 (Figure4). The transmission line 506 includes a quarter wave section 502. The quarter wave section ("QWS") 502 is a transmission line which is a quarter-wavelength long at the lowest operational frequency. The QWS 502 can include transmission line elements or discrete components. It is preferred that the QWS 502 have small size and low insertion loss. The parallel circuit 500, in a preferred embodiment, is formed on a substrate, such as a semiconductor substrate. The parallel circuit 500 includes four "T" shape RLC circuits, three diode circuits, and two variable impedance circuits (Z circuits). The compensation circuits ("CMP") are optional impedance compensation circuits that are required only to optimize the off state PIN diode impedance over multiple frequency bands. The three diodes, D1, D2, D3, are preferably PIN diodes.

The transmission line 506 extends between a signal source (e.g. a radio) and an antenna. The radio can transmit or receive one or more of a variety of radio frequency signals. For example, the radio may transmit on a first frequency range and receive on a second frequency band. The three control inputs are labeled "Select 1", "Select 2", and "Enable" and they control the operation of the parallel circuit 500 as described in Table 1.

When the parallel circuit 500 is in the transmission mode, the signal (e.g. radio frequency energy) passes from the radio node to the antenna node with a low insertion loss and high linearity. In the transmission mode, the quarter wave section ("QWS") 502 provides a low insertion loss and the quarter wave termination circuit ("QWT circuit") 504 provides high impedance with high linearity. In the transmission mode, it is preferred that the QWS 502 mirror the

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characteristics of a 50 ohm transmission line. In a preferred embodiment, the QWS 502 has an insertion loss below 0.30 dB at 2 GHz.

In the transmission mode, the QWT circuit 504 is not biased and provides a low loss and high linearity. Low loss exists when the QWT circuit 504 provides a high "off" state impedance. High linearity is defined as having second and third order intercept points that are substantially infinite. For design reasons, low loss levels and high linearity are traded off. It is preferred that the QWT 504 have an insertion loss of less than 0.15 dB at 2 GHz. When in the transmission mode (thru mode), it is preferred that the QWT 504 should have an insertion loss of less than 0.55 dB.

In the transmission mode, the three control inputs are allowed to float and thus, the diodes, D1, D2, D3, are not biased. Since the QWT is a parasitic impedance to ground, the PIN diode off state impedance dominates the overall transmission mode insertion loss. As the diode's off state impedance increases, the overall network loss decreases. If PIN diodes are used, a high impedance parallel RLC circuit will result. The QWT circuit 504 acts as a parasitic impedance to ground, causing the PIN diode off state impedance to dominate the transmission mode insertion loss. As the diode off state impedance increases, the loss decreases. The two optional impedance compensation circuits labeled "CMP" in Figure 5 are used to optimize the off state PIN diode impedance over multiple frequency bands. The QWT 504 illustrated in Figure 5 does not require a reverse bias voltage.

In conventional systems, such as applications used for the Global System for Mobile telecommunication ("GSM") standard, shunt PIN diodes require a reverse bias voltage to prevent peak RF voltages from turning on the shunt diodes. If the shunt PIN diode turns on during the RF power transmission, the diodes drain the current from the transmission signal. This can result in the creation of numerous undesirable spurious radio frequency artifacts. Two methods can prevent the shunt diodes from turning on. First, traditional systems use a large reverse bias voltage applied to the PIN diode to ensure it does not turn on. Second, the parallel circuit prevents the radio frequency voltage from reaching the

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return path to ground. The QWT circuit 504 prevents the radio frequency from reaching the ground path by providing anode-to-anode diode configurations, D1 to D2 and D1 to D3, coupled with the "T" bias circuits (RLC circuits).

D1 of Figure 5 will turn on when the current flows through D2, D3 or the second RLC "T" bias circuit (L2, R2, C2). An embodiment of D1 is shown in Figure 3 as a switch 310. That is, D1 is turned n when a positive voltage is applied to the "Enable" input. Since D1 is orientated anode-to-anode with respect to D2 and D3, D1 will not turn on simultaneously with D2 or D3 when a peak negative radio frequency voltage is transmitted on the transmission path 506. Thus, the only current path to ground for the peak negative voltage is through the first RLC "T" circuit (L1, R1, C1). The inductors L1, L2, L3, and L4 are high impedance radio frequency chokes. The chokes (L1, L2, L3, and L4) prevent the radio frequency current from finding a return path to ground. The capacitors C2, C3, C4, reference one end of the radio frequency chokes L2, L3, L4, respectively, to ground. This prevents performance anomalies resulting from the bipolar driver transistor parasitics.

The QWT circuit 504 provides numerous advantages over existing series tuning circuits. For example, in the transmission mode (thru mode) the QWT circuit 504 drains no current and provides increased linearity. A series PIN circuit requires up to 10 mA (GSM at 2 Watts) to optimize insertion loss and linearity. Some low loss PIN diodes are currently manufactured using an "Epi" process and high linearity diodes are manufactured using a less expensive "bulk" process.

The second mode of operation for the QWT circuit 504 is the "isolation mode", also called isolation band mode. The isolation mode presents a specific impedance at the antenna feed point. The impedance is selected to optimize the antenna-to-antenna isolation. It is preferable that the impedance be digitally selectable. In a preferred embodiment, the selection is dynamic, adapting to changes in the environment. The method of selecting the appropriate impedance is called quarter wave matching. The impedance looking into a quarter wave section is a function of the quarter wave section output port termination. If the output port is terminated in a zero Ohm impedance (a short to ground), the impedance seen at

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the quarter wave section input port is extremely high, that is an open circuit, at that specific frequency. If the output port is terminated in a high impedance, that is an open circuit, the impedance seen at the quarter wave input port is extremely low, that is a short.

The QWS 502 terminating impedance is selected by applying a bias voltage at both the "enable" node and one of the two "select" nodes, Select 1 and Select 2. The bias voltage turns on PIN diode D1 and one, but not both PIN diodes D2 and D3. The diodes are used to select the desired QWS 502 termination impedance. As variable impedance circuit Z1 or Z2 increase in inductance, the QWS 502 input reflection coefficient position rotates clockwise on the Smith chart (not shown), a circular graphical device commonly used in the industry. The variable impedance circuits Z1 and Z2 can include inductance and/or capacitance circuits. As variable impedance circuit Z1 or Z2 decrease in inductance, the QWS 502 input reflection coefficient position rotates counter clockwise on a Smith chart. As the QWS 502 input reflection coefficient changes position on the Smith chart, the associated impedance is scaled.

The relationship between the reflection coefficient ρ v looking into the QWS 502 from the antenna and the input impedance Zin at the same location is given by Equation 1.

$$Zin = (Zo * (\rho v + 1)) / (1 - \rho v)$$

Eqn. 1

Zin is the input impedance

Zo is the system characteristic impedance

Ov is the reflection coefficient

The QWS 502 scales the termination impedance at the desired frequency.

The QWS 502 is designed to be a quarter wave circuit at the lowest operational frequency band. If isolation is desired in the lowest operational frequency band, a large capacitor is used for the Z1 termination. A capacitor that acts as a short circuit at radio frequencies is called a RF short. If a RF short is used to terminate the input port of a QWS 502, the output port impedance will have an

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extremely high impedance, that is effectively an open. The output port of the QWS 502 is the end closest to the antenna and the input port is the end closest to the radio. As the operational frequency increases, Z1 will not terminate the QWS 502 in the proper impedance. The problem is that the electrical length of the QWS 502 becomes too long as the operational frequency increases. To correct this problem, the Z2 termination impedance is switched on to normalize the QWS 502 electrical length. After normalization, the QWS 502 input port has a high impedance in the desired frequency range.

The resolution of the impedance selection is a function of the number of network stages. Higher resolution requires more stages.

This parallel circuit 504, also called a termination stage, can be used on a single antenna in a multiple antenna system or more than one antenna in the multiple antenna system. In a preferred embodiment, every antenna in a multiple antenna system is connected with a parallel circuit 504.

The parallel circuit 504 provides several advantages over the existing systems. First, the impedance is digital selectable via the Enable, Select 1, and Select 2. Second, the parallel circuit 504 can isolate multiple bands without requiring a negative voltage bias to control the transmission mode linearity. This reduces the circuit complexity and size, and costs. Third, the multiple band isolation mode eliminates the need for multiple quarter-wave sections. This reduces the circuit complexity and size, and costs. Fourth, the termination impedance can be implemented with discrete components. Fifth, optimum antenna termination impedance for multiple frequency bands can be selected via the control signals. Sixth, the frequency bandwidth and tuning resolution can be modularly extended with additional termination stages.

While preferred embodiments have been shown and described, it will be understood that they are not intended to limit the disclosure, but rather it is intended to cover all modifications and alternative methods and apparatuses falling within the spirit and scope of the invention as defined in the appended claims or their equivalents.

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WHAT IS CLAIMED IS:

- 1.A multiple antenna system, comprising:
- (a) first and second antennas;
- (b) first and second signal circuits connected with respective first and second antennas via first and second signal paths;
- (c) a first parallel tuning circuit selectively connectable in parallel with the first signal path, the first tuning circuit selectively adjusting the impedance of the first antenna.
- 2. The multiple antenna system of claim 1 further comprising a third antenna connected with a third signal source via a third signal path.
- 3. The multiple antenna system of claim 1, wherein the first and second signal circuits are capable of generating electromagnetic signals.
- 4. The multiple antenna system of claim 3, wherein the electromagnetic signals include radio frequency signals.
- 5. The multiple antenna system of claim 1, wherein the first and second signal circuits generate signals at unique frequencies.
- 6. The multiple antenna system of claim 1, wherein the first and second signal circuits generate signals at the same frequencies.
- 7. The multiple antenna system of claim 1, wherein the first and second antennas are fabricated on a common dielectric material.
- 8. The multiple antenna system of claim 1, further comprising an antenna housing capable of housing at least the first and second antennas.
- 9. The multiple antenna system of claim 1, wherein the second signal circuit is capable of generating signals in multiple frequency bands.

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- 10. The multiple antenna system of claim 9, wherein the first parallel tuning circuit is capable of increasing isolation between the first and second antennas in multiple frequency bands.
- 11. The multiple antenna system of claim 1, wherein the first parallel tuning circuit includes an impedance matching circuit.
- 12. The multiple antenna system of claim 11, wherein the impedance matching circuit is capable of matching an impedance of the second antenna via electromagnetic coupling with the first antenna.
- 13. The multiple antenna system of claim 11, wherein the impedance matching circuit is capable of matching an impedance of the second antenna.
- 14. The multiple antenna system of claim 11, wherein the first tuning circuit includes a plurality of impedance matching circuits, each impedance matching circuit being independently selectively connectable in parallel to the first signal path.
- 15. The multiple antenna system of claim 1 further comprising:(d) a second parallel tuning circuit selectively connectable to the second signal path.
- 16. The multiple antenna system of claim 15, wherein the second parallel tuning circuit is capable of optimizing isolation between the first and second antenna.
- 17. The multiple antenna system of claim 1, wherein the first tuning circuit is selectively connectable to the first signal path near the first antenna.
- 18. The multiple antenna system of claim 1, wherein the first tuning circuit creates an impedance at an input of the first antenna substantially equivalent to an open circuit at the transmission frequency of the second antenna.

- 19. The multiple antenna system of claim 1, wherein the first parallel tuning circuit includes a plurality of band tuning circuits, each band tuning circuit being independently selectively connectable with the first signal path.
- 20. The multiple antenna system of claim 19, wherein each band tuning circuit creates a different impedance at an input to the first antenna.
- 21. The multiple antenna system of claim 19, wherein the first tuning circuit includes a first band tuning circuit capable of tuning the second antenna and a second band tuning circuit capable of tuning a third antenna.
- 22. The multiple antenna system of claim 19, wherein the first parallel tuning circuit is capable of dynamically adjusting the impedance.
- 23. The multiple antenna system of claim 19, further comprising a detector capable of dynamically connecting one or more of the plurality of band tuning circuits with the first signal path.
- 24. The multiple antenna system of claim 1, wherein the first signal source includes a radio transceiver.
 - 25. The multiple antenna system of claim 1, wherein the multiple antenna system is adaptable for use in a cellular telephone.
 - 26. A parallel tuning circuit for use in a multiple antenna system, comprising:
 - (a) a first impedance matching circuit; and
- (b) a first switch capable of selectively connecting in parallel the first impedance matching circuits with a first antenna.
 - 27. The parallel tuning circuit of claim 26, further comprising
 - (c) a second impedance matching circuit; and
 - (d) a second switch capable of selectively connecting in parallel the second impedance matching circuits with a second antenna.
 - 28. The parallel tuning circuit of claim 26, wherein the first impedance matching circuit is capable of matching an impedance of a second antenna.

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- 29. The parallel tuning circuit of claim 26, wherein the first impedance matching circuit is capable of matching an impedance in multiple frequency bands.
- 30. The parallel tuning circuit of claim 26, wherein the first impedance matching circuit includes a selectable impedance.
- 31. The parallel tuning circuit of claim 30, wherein the selectable impedance is digitally selectable.
- 32. The parallel tuning circuit of claim 30, wherein first impedance matching circuit dynamically adjusts impedance based on external interference.
- 33. A method of adjusting impedance in a multiple antenna system, comprising:

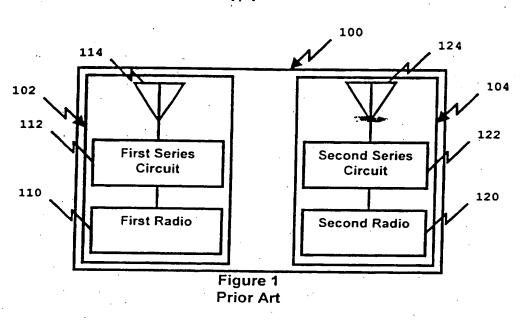
 (a) detecting a first operational state of a first signal source connected with a first antenna via a first signal path;
- (b) detecting a second operational state of a second signal source, the second signal source being connected with a second antenna via a second signal path, the second antenna being located near the first antenna; and
- (c) selectively connecting a parallel impedance circuit with the first signal path based on the first and second operational states.
 - 34. The method of claim 33, further comprising:
- (d) measuring external interference near the first antenna; and
- (e) automatically adjusting the parallel impedance circuit based on the external interference.
- 35. The method of claim 33, wherein (b) includes detecting an operational state of a third signal source, the third signal source being connected with a third antenna via a third signal path, the third antenna being located near the first antenna and (c) includes connecting a parallel impedance circuit with the first signal-path based-on-the first, second, and third operational states.
- 36. The method of claim 33, wherein (c) includes selectively attaching one of a plurality of parallel impedance circuits with the first signal path.

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- 37. The method of claim 33, further including (d) selectively attaching a second parallel impedance circuit with the second signal path.
- 38. The method of claim 33, wherein (c) includes selecting a desired parallel impedance, selecting from a plurality of parallel impedance circuits a parallel impedance circuit that most closely matches the desired parallel impedance, and attaching the selected parallel impedance circuit with the first signal path.

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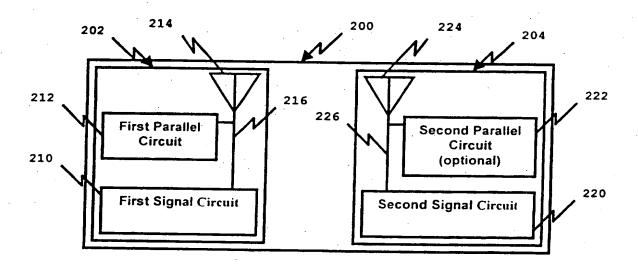


Figure 2

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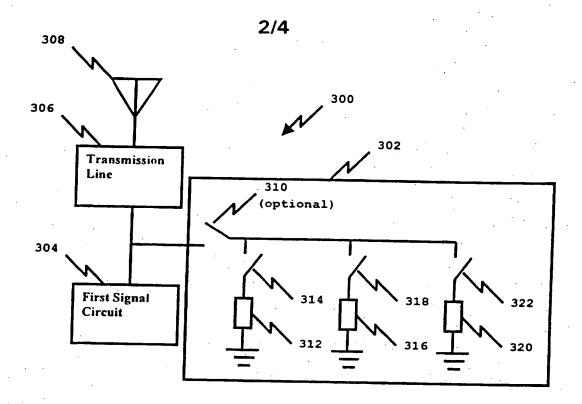


Figure 3

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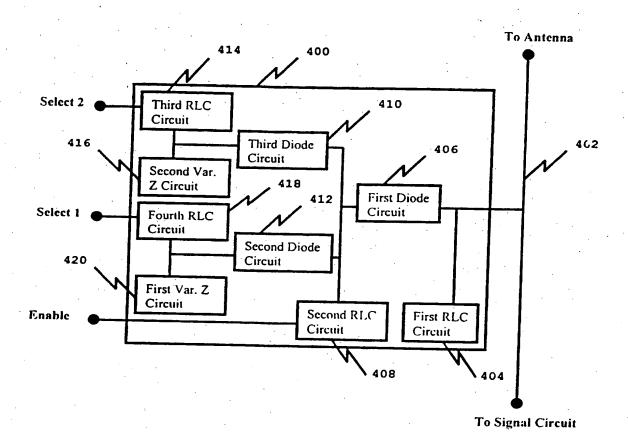
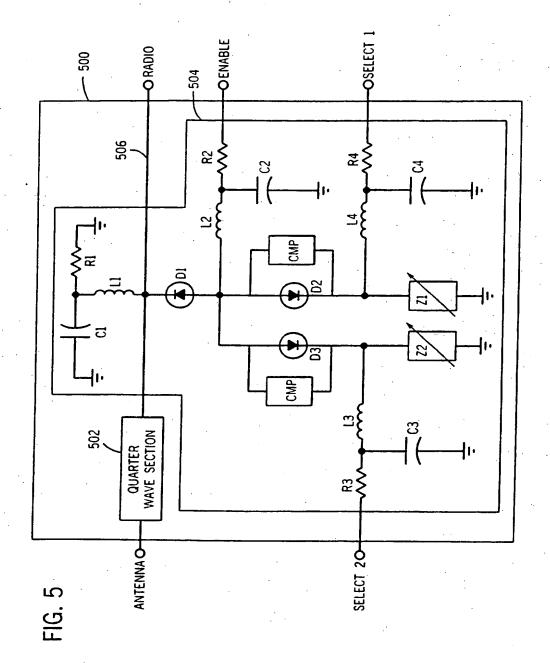


Figure 4

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INTERNATIONAL SEARCH REPORT

Interna. J Application No PCT/US 01/08693

CLASSIFICATION OF SUBJECT MATTER
PC 7 H0101/24 H010 IPC 7 According to International Patent Classification (IPC) or to both national classification and IPC B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC 7 H01Q H03H Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data, PAJ, INSPEC C. DOCUMENTS CONSIDERED TO BE RELEVANT Relevant to claim No. Citation of document, with indication, where appropriate, of the relevant passages Category 1 - 32US 4 806 944 A (JACOMB-HOOD ANTHONY W) X 21 February 1989 (1989-02-21) 33 the whole document 1,26,33 EP 0 680 161 A (NIPPON ELECTRIC CO) 2 November 1995 (1995-11-02) column 1, line 41 - line 50 column 5, line 8 - line 20; figure 1 34,35 US 4 233 607 A (SANFORD GARY G ET AL) Α 11 November 1980 (1980-11-11) cited in the application column 4, line 43 - line 61; figure 2 1,26,33 EP 0 465 315 A (MATRA COMMUNICATION) 8 January 1992 (1992-01-08) column 2, line 34 - line 58 column 3, line 1 - line 28 Patent family members are listed in annex. Further documents are listed in the continuation of box C. Special categories of cited documents: *T* later document published after the international filing date or pnorty date and not in conflict with the application but cited to understand the principle or theory underlying the A document defining the general state of the art which is not considered to be of particular relevance invention "E" earlier document but published on or after the international document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone titing date *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such docu-O document referring to an oral disclosure, use, exhibition or ments, such combination being obvious to a person skilled in the art. other means *P* document published prior to the international filling date but "&" document member of the same patent family later than the priority date claimed Date of mailing of the international search report Date of the actual completion of the international search 06/09/2001 29 August 2001 Authorized officer Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl. Moumen, A Fax: (+31-70) 340-3016

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